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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,382	03/03/2005	Barry H. Harrison	21854-00051-US1	3838

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EXAMINER	
LAM, DAVID	
ART UNIT	**PAPER NUMBER**
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,382	HARRISON ET AL.	
	Examiner	Art Unit	
	David Lam	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-3,11,12,14-20 and 22-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-10,13 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/05,11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election of claims 4-10, 13, 21 in the reply filed on 12/13/06 are acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 1-3, 11-12, 14-20, 22-24 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/13/06.

Patentable Weight

2. The recitation of "the capacitor" has not been given patentable weight because the recitation occurs in a negative statement.

Drawings

3. Figures 1a-c should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 4- 5 are objected to because of the following informalities:

- In claim 4, the phrase "in which a silicon carbide device is substituted for the capacitor between the control gate and floating gate" should be change to -- in which a silicon carbide device disposed between a control gate and floating gate --;
- In claim 5, "a diode" should be change to – an isolation diode --, in order to be constant with the isolation diode in claim 13;
- In claim 21, applicant should delete -- or a MOSFET as claimed in claim 16 --, since claim 16 not in the elected group of claims. Appropriate correction is required.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 4, 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4, recites the limitation "the control gate" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recited the limitation " information is read by sensing resistance between the source and drain terminals of the transistor" is unclear, the Examiner does not understand what information is read form where?

Claims 8, recites the limitation "the SIC-SIO_2 interface" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim 13, recites the limitation "with both forward and reverse on operation when the forward and reverse turn-on voltages are exceeded." is unclear, the Examiner does not understand what operation? and voltage are exceeded what voltage?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4-5, insofar as in compliance with *35 USC § 112,* are rejected under 35 U.S.C. 102(e) as being anticipated by Mikami et al. (6,344991).

Regarding to claims 4- 5, Mikami et al. disclose a dynamic nonvolatile RAM comprising one transistor cells in which a silicon carbide device (2) formed between control gate and floating of the transistor and information is read by sensing resistance between the source and drain terminals of the transistor (See at least Col. 3, lines 33-65), wherein the silicon carbide device is a diode. *See at least Figs. 60-63, for example of Cols. 13-15, lines 64-67, 1-67, 1-52 and the related disclosure.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6, 13 insofar as in compliance with *35 USC § 112,* rejected under 35 U.S.C. 103(a) as being unpatentable over Mikami et al. (6,344991).

With respect to claim 6, Mikami et al. disclose all the elements as applied to claim 4 above.

Mikami et al. not explicitly disclose where the silicon carbide device is a controlled switch, it would have been inherently include, if not, the use of silicon carbide as a control switch would have been known and available in art to handling high voltages and/or large currents. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Mikami et al. accordingly in order to provide efficiency and reliable switching control in a semiconductor memory device. *NOTE: Col. 1, line 45-61 of Das et al. (6,972,436) cited to support known position.*

With respect to claim 13 as understood by Examiner, Mikami et al. disclose all the elements as applied to claim 5 above.

Mikami et al. not explicitly disclose wherein the isolating diode is a reference type diode with both forward and reserve bias direction to turn on a voltage, it would have been inherently included (Zener diode), if not, forming a reference type diode with both forward and reserve bias direction to turn on a voltage would have been known and available in the art to enhanced noise tolerance. It would have been obvious to on having ordinary skill in the art at the time of the invention to modify Mikami et al. accordingly in order to reduce power consumption, noise with in a semiconductor memory device. *NOTE: for example of at least Cols. 18-19, lines 50-67, 1-19 of Rockett (6,429,492) cited to support known position.*

9. Claims 7, 9 insofar as in compliance with *35 USC § 112,* rejected under 35 U.S.C. 103(a) as being unpatentable over Mikami et al. (6,344991) in view of Soref et al. (5,880,491).

With respect to claim 7, Mikami et al. disclose all the elements as applied to claim 4 above.

Mikami et al. fail to specify where in the silicon carbide is a 3C SiC wafer.

Soref et al. disclose a semiconductor memory device comprising 3C SiC wafer (41 or 3').

It would have been obvious to one having ordinary skill in the art at the time of the invention to provide a 3C SiC wafer of Mikami et al. as taught by Soref et al. in order to provide high reliable and low cost wafer in semiconductor memory device.

With respect to claim 9, the proposed invention of Mikami et al. and Soref et al. disclose all the elements as applied to claim 7 above.

Mikami et al. and Soref et al. lack an inclusion of wherein the charge retention times are greater than 7 years. The use of forming a semiconductor with charge retention times are greater than 7 years would have been know and available in the art to improved the relability. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Mikami et al. and Soref et al. to accordingly by provide charge retention times that is greater than 7 years in order improved reliability and lower power consumption. *NOTE: for example of at least Col. 8, lines 1-15 of Forbes et al. (6,965,123) cited to support known position.*

10. Claims 8, 10 insofar as in compliance with *35 USC § 112,* rejected under 35 U.S.C. 103(a) as being unpatentable over Mikami et al. (6,344991) in view of Forbes et al. (6,965,123).

With respect to claim 8, Mikami et al. disclose all the elements as applied to claim 5 above.

Mikami et al. lack an inclusion of wherein the diode is implemented in silicon carbide with SIC-SIO_2 interface passivated to created charge retention times sufficiently long to avoid the need for the 1T memory cell to be electrically refreshed.

Forbes et al. disclose a memory device comprising silicon carbide with SIC-SIO_2 interface passivated to created charge retention times sufficiently long to avoid the need for the 1T memory cell to be electrically refreshed. *See at least Fig. 10, for example of Cols. 11-12, lines 61-67, 1-4, respectively; Col. 15, lines 30-44 and the related disclosure.*

It would have been obvious to one having ordinary skill in the art at the time of the invention to provide silicon carbide with SIC-SIO_2 interface passivated to created charge retention times sufficiently long to avoid the need for the 1T memory cell to be electrically refreshed of Mikami et al.'s diode as taught by Forbes et al. in order to improved reliability, low power consumption and extend life time of the semiconductor memory device.

With respect to claim 10, the proposed invention of Mikami et al. and Forbes et al. disclose all the elements as applied to claim 8 above.

Mikami et al. and Forbes et al. lack an inclusion of wherein the SIC-SIO_2 interface is nitrided in either NO or N_2O rich environment. Forming a SIC-SIO_2 interface is nitrided in either NO or N_2O rich environment would have been known and available in the art to provide low melting or low disassociation temperatures. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Mikami et al. and Forbes et al. to

provide SIC-SIO_2 interface is nitrided in either NO or N_2O rich environment in order to highly reliable and low cost semiconductor memory device. *NOTE: for example of at least Col. 4, lines 31-49 cited to support known position.*

11. Claim 21 insofar as in compliance with *35 USC § 112,* rejected under 35 U.S.C. 103(a) as being unpatentable over Mikami et al. (6,344991) and Forbes et al. (6,965,123) as applied to claim 10 above, and further in view of Chu (7,145167).

With respect to method claim 21, Mikami et al. and Forbes et al. disclose all the elements as applied to claim 10 above.

Mikami et al. and Forbes et al. lack an inclusion of a method of fabricating the NVRAM comprising steps of forming a nitrided silicon oxide gate on the silicon carbide substrate and subsequently carrying out the ion implantation and then finishing the formation of the MOSFET.

Chu discloses a method of fabricating the NVRAM comprising steps of forming a nitrided silicon oxide gate (111 or 121) on the silicon carbide substrate (11) and subsequently carrying out the ion implantation and then finishing the formation of the MOSFET. *See at least Figs. 11-12, for example of Cols. 7, 14, line 13-29, lines 9-46, respectively and the related disclosure.*

It would have been obvious to one having ordinary skill in the art at the time of the invention to provide a method of fabricating of Mikami et al. and Forbes et al. comprising steps of forming a nitrided silicon oxide gate on the silicon carbide substrate and subsequently carrying out the ion implantation and then finishing the formation of the MOSFET as taught by Chu in order to provide high-speed and low noise semiconductor memory device.

Allowable Subject Matter

12. Claim XX objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach XXX.

13. The following is an examiner's statement of reasons for allowance: Claims XX are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Forbes et al. (6,794,255) disclose carburized silicon gate insulators for integrated circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAVID LAM
PRIMARY EXAMINER

D. Lam

February 12, 2007